UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

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First Named Inventor or Application Identifier	
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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☐ Fee Transmittal Form
   (Submit an original, and a duplicate for fee processing)
2. [x] Specification [Total pages 7]
   5 pages description
   1 pages abstract
   1 pages claims
   3 claims
3. [x] Drawing(s) *(35 USC 113)* [Total sheets 2]
   ☐ Informal [x] Formal [Total drawings 7]
4. ☐ Oath or Declaration [Total pages]
   a. ☐ Newly executed (original or copy)
   b. ☐ Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 17 completed)
   [Note Box 5 below]
   i. ☐ DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation by Reference
   (usable if Box 4b is checked)
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Microfiche Computer Program (Appendix)
7. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   a. ☐ Computer Readable Copy
   b. ☐ Paper Copy (identical to computer copy)
   c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☐ Assignment Papers (cover sheet & documents(s))
9. ☐ 37 CFR 3.73(b) Statement ☐ Power of Attorney
   (when there is an assignee)
10. ☐ English Translation of Document *(if applicable)*
11. [x] Information Disclosure Statement (IDS)/PTO-1449 [x] Copies of IDS Citations
12. ☐ Preliminary Amendment
13. [x] Return Receipt Postcard (MPEP 503)
    (Should be specifically itemized)
14. ☐ Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired
15. ☐ Certified Copy of Priority Document(s)
    (if foreign priority is claimed)

16. Other: PURSUANT TO 35 U.S.C. §119, APPLICANT HEREBY CLAIMS PRIORITY TO FRENCH PATENT APPLICATION 98 09801, FILED JULY 28, 1998

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.:

☐ Cancel in this application original claims of the prior application before calculating the filing fee.

☐ Amend the specification by inserting before the first line the sentence:

This application is a ☐ continuation ☐ divisional of application serial no. , filed , entitled , and now .

18. CORRESPONDENCE ADDRESS

Correspondence address below

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19. SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED	
NAME	James H. Morris, Reg. No. 34,681
SIGNATURE	
DATE	July 27, 1999

IMAGE SENSOR WITH A PHOTODIODE ARRAY

Background Of The Invention

1. Field of the Invention

The present invention relates to the field of image sensors, usable for example in video cameras.

2. Discussion of the Related Art

Among the various techniques for converting an image projected on a target into electric data, targets formed of a semiconductor substrate supporting an array of photodiodes are used. The diodes are generally reverse-biased and capacitively charged. In the absence of light, they keep their charge and, when lit, they discharge. A bright image element or pixel can thus be differentiated from a dark pixel and an image in the form of a matrix of data corresponding to the electric charges of each of the pixels can thus be restored.

Further, it is known to form this matrix so that all pixels are divided into three sub-arrays corresponding to each of three colors (currently, red, green, and blue). For this purpose, each of the pixels, that is, each of the diodes, is coated with a color filter. It is known to use an interference filter as a color filter. Interference filters formed of materials compatible with usual MOS-type integrated circuit manufacturing lines have also been provided. Thus, an interference filter may be formed of a silicon oxide layer coated with a polysilicon layer, itself coated with a silicon nitride layer. In fact, the successive materials have to alternately have low and high optical indexes.

In such structures, the storage capacity of each pixel is associated with the pixel dimension and more specifically with the dimension of the junction of the associated diode.

Summary Of The Invention

An object of the present invention is to increase this storage capacity without increasing the dimension of an elementary cell of the sensor and without complicating its manufacturing.

To achieve this object as well as others, the present invention provides an array of photodiodes formed of regions of a second conductivity type formed in a semiconductive region of a first conductivity type, divided into three interleaved sub-arrays, all the photodiodes of a same sub-array being coated with a same interference filter including at least one insulating layer of determined thickness coated with at least one conductive layer. The conductive layers are electrically connected to the semiconductive region of a first conductivity type.

According to an embodiment of the present invention, the electric connection is indirect.

According to an embodiment of the present invention, the semiconductor substrate is a single-crystal silicon substrate, and the interference filter includes a silicon oxide layer formed above the substrate and a conductive polysilicon layer formed above the silicon oxide layer.

The foregoing objects, features and advantages of the present invention will be discussed in detail in the following non-limiting description of specific embodiments in connection with the accompanying drawings.

Brief Description Of The Drawings

Fig. 1A shows a simplified cross-sectional view of a pixel of a photodiode array according to the present invention;

Fig. 1B shows the equivalent diagram of the pixel of Fig. 1A;

Figs. 2A, 2B, 2C illustrate successive steps of a method of realization of a layer of an interference filter used according to the present invention;

Fig. 3 shows in the form of a diagram an image sensor formed of a photodiode matrix according to the present invention; and

Fig. 4 shows an example of realization of a pixel of an image sensor according to Fig. 3.

Detailed Description

It should be noted that, as usual in the field of the representation of semiconductor components, the various drawings are not drawn to scale but that the dimensions of their various elements have been arbitrarily modified to facilitate the readability and simplify the drawing.

Fig. 1A shows a cross-sectional view of a photodiode associated with an interference filter according to the present invention. This photodiode is formed of an N-type semiconductive region 1 formed in a P-type semiconductor substrate 2. It will be assumed herein that the substrate is made of single-crystal silicon. Above region 1 is formed a multiple layer deposition forming an interference filter and including, for example, a silicon oxide layer 4, a polysilicon layer 5, and a silicon nitride layer 6. For optical radiation in the visible field, single-crystal silicon and polysilicon have a high refraction coefficient, on the order of 4, while silicon oxide and silicon nitride have low coefficients, on the order of 1.5. In a known manner, the thicknesses of the different layers have to be adjusted to have a coated effect and a filtering effect adapted to a specific wavelength. For example, if layers 5 and 6 have respective thicknesses of 20 and 50 nm, a filter is formed for blue by choosing for oxide layer 4 a thickness on the order of 150 nm, a filter is formed for green with

a thickness on the order of 190 nm, and a filter is formed for red with a thickness on the order of 230 nm.

According to the present invention, polysilicon layer 5 is not left floating but is set to the same potential as substrate 2. This is schematically illustrated in the drawing by a contact between layer 5 and a heavily-doped P-type region 8 of substrate 2. Polysilicon layer 5 is sufficiently doped to be well conductive; it may also be coated with a metal layer (aluminum) or be silicided, outside regions where it is useful to make a filter.

Due to the link between layer 5 and substrate 2, the structure corresponds to the equivalent diagram shown in Fig. 1B. It is assumed that cathode region 1 of photodiode D is connected to a terminal K not shown in Fig. 1A and that the anode of the photodiode is connected to a terminal A, currently grounded. The presence of conductive layer 5 connected to the substrate is equivalent to the existence of a capacitor C arranged in parallel on the diode. The first "plate" of the capacitor is formed of layer 5 connected to the substrate, that is, to the diode anode. The second "plate" of the capacitor corresponds to cathode region 1 of the diode.

The equivalent capacity of each diode is thus increased, that is, the storage capacity of each photoelement and thus, the dynamics of the electric signals resulting from a lighting, is increased. The linearity of the charge/voltage characteristic is also improved by adding a constant capacitance to the capacitance of the diode junction which is variable with the applied voltage.

Figs. 2A to 2C illustrate an example of a method for forming oxide layers of different thicknesses over three groups of cathode regions 1R, 1G, 1B respectively sensitive to red, to green, and to blue.

In a first step illustrated in Fig. 2A, a first silicon oxide layer 4-1 is deposited and etched to maintain it in place only above regions 1R.

In a second step illustrated in Fig. 2B, a second silicon oxide layer 4-2 is deposited and etched to only leave it in place above regions 1R and 1G.

In a third step illustrated in Fig. 2C, a third silicon oxide layer 4-3 is deposited and left in place. After this, a polysilicon layer 5 and possibly, as previously described, a silicon nitride layer, are deposited. Then, the structure is properly etched to enable making contacts at selected locations.

The thickness of layer 4-3, in the case of the example given previously, is 150 nm, and the thicknesses of layers 4-1 and 4-2 are 40 nm so that oxide layers having respective thicknesses of 230, 190 and 150 nm are found above regions 1R, 1G, and 1B.

Fig. 3 partially shows as an example and in the form of a circuit the conventional structure of a

photodiode array intended for forming an image sensor. Each photodiode Dij is connected by its anode to the ground and by its cathode to the source of a precharge transistor Pij, the drain of which is connected to a reference voltage VR and the gate of which is connected to a row line Ri meant to select all the transistors Pij of a same row. Thus, in a first phase, diodes Dij are precharged. Then, after lighting, the voltage across the diodes is read by means of an amplifier formed, for example, of a first transistor Tij, the gate of which is connected to the connection node of transistor Pij and diode Dij, the source of which is connected to a column line Cj and the drain of which is connected to a high voltage Vdd. Each line Cj is connected to an amplifier Aj forming for example with transistor Tij a follower amplifier.

In such a structure, each diode Dij can be of the type described in connection with FIGS. 1A-1B, that is including a diode in parallel with a capacitor (not shown in FIG. 3).

An example of realization of a precharge transistor Pij and of a diode Dij is illustrated in Fig. 4. This structure is formed in a P-type single-crystal silicon substrate 10. Each transistor Pij includes an N-type drain region 11 and an N-type source region 12. Source region 12 extends to form the cathode region of diode Dij, the anode of which corresponds to substrate 10. Between the drain and the source of transistor Pij is formed an insulated gate 13, for example, made of polysilicon. The interference filter structure including layers 4, 5, and 6 already described in relation with Fig. 1 extends above most of region 12. Drain region 11 forms one piece with metallization 15 establishing a contact with a precharge voltage source VR.

Source/cathode region 12 forms one piece with a metallization 16 connected to the gate of transistor Tij (see Fig. 3). Further, and according to the present invention, polysilicon region 5 is connected to substrate 10. More currently, each of these regions will be connected to a common ground.

According to an alternative of the present invention, the diodes can be formed in a well itself formed in a substrate, that is, considering Fig. 4, P region 10 is a well formed in an N-type substrate not shown. In this case, polysilicon region 5 can be connected to the substrate and not directly to region 10.

Of course, the present invention is likely to have various alterations, modifications, and improvements which will readily occur to those skilled in the art. In particular, the various described materials may be replaced with equivalent materials. Other materials compatible with the manufacturing of semiconductor components may be used to make the interference filter formed above each diode. A significant feature of the present invention is that one layer of this interference

filter, separated from the semiconductor substrate by an insulating layer, is conductive and is connected to the substrate. All the described types of conductivity may be inverted. Further, although a silicon substrate has been described, it should be noted that other semiconductor systems may be adapted to the implementation of the present invention.

Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is:

CLAIMS

1. An array of photodiodes made of regions of a second conductivity type formed in a semiconductive region of a first conductivity type, divided into three interleaved sub-arrays, all the photodiodes of a same sub-array being coated with a same interference filter including at least one insulating layer of determined thickness coated with at least one conductive layer, wherein said conductive layers are electrically connected to the semiconductive region of a first conductivity type.

2. The array of photodiodes of claim 1, wherein the electric connection is indirect.

3. The array of photodiodes of claim 1, wherein the semiconductor substrate is a single-crystal silicon substrate, and the interference filter includes a silicon oxide layer formed above the substrate and a conductive polysilicon layer formed above the silicon oxide layer.

ABSTRACT

An array of photodiodes includes regions of a second conductivity type formed in a semiconductive region of a first conductivity type, divided into three interleaved sub-arrays. All the photodiodes of a same sub-array are coated with a same interference filter including at least one insulating layer of determined thickness coated with at least one conductive layer. According to the present invention, the conductive layers are electrically connected to the semiconductive region of a first conductivity type.

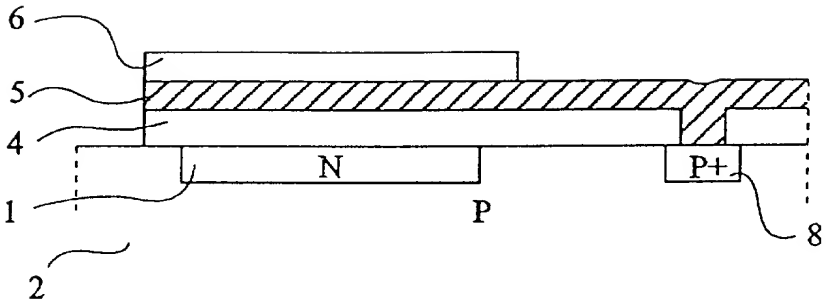

Fig 1A

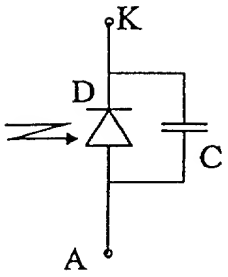

Fig 1B

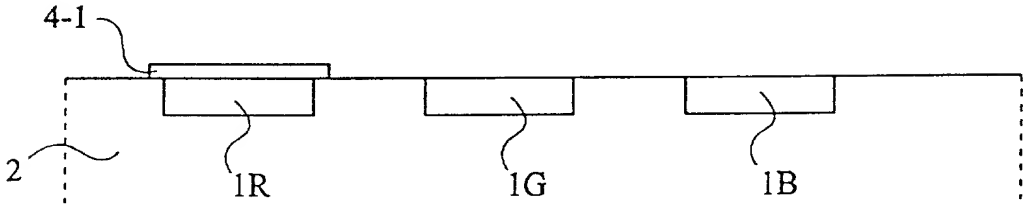

Fig 2A

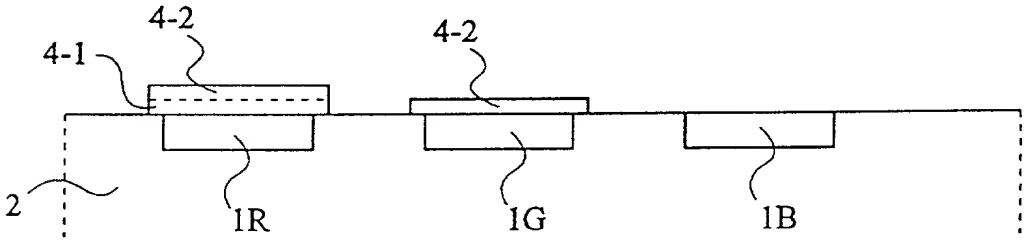

Fig 2B

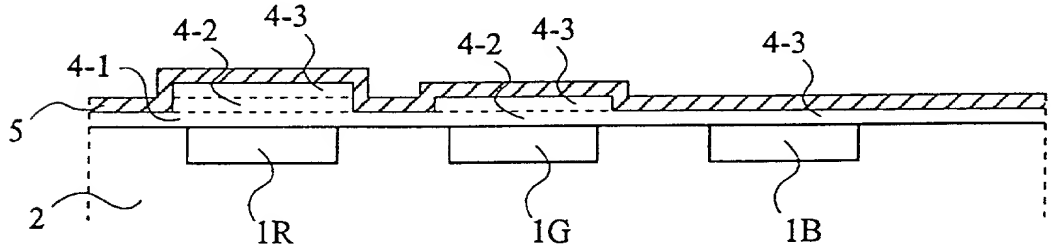

Fig 2C

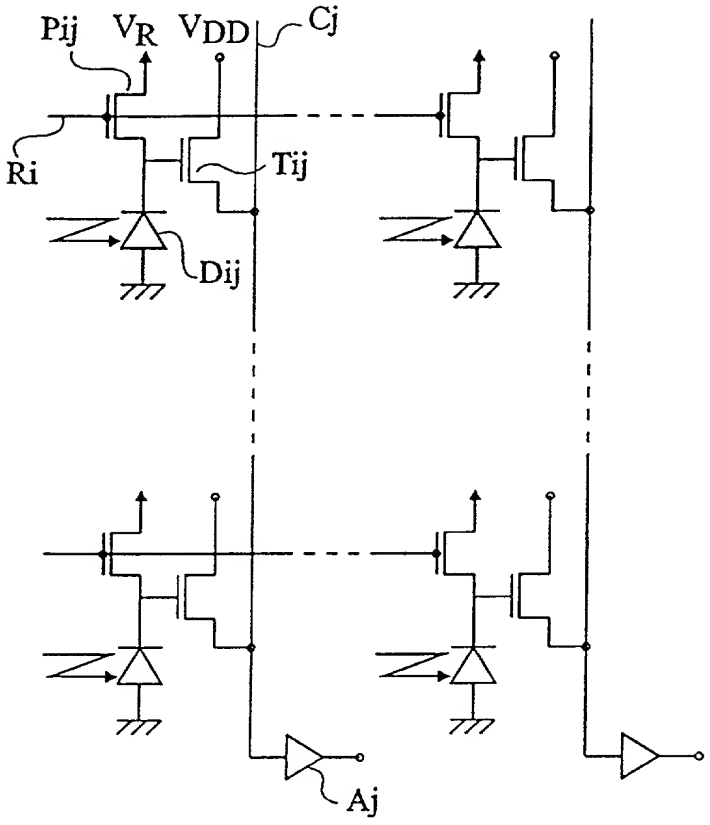

Fig 3

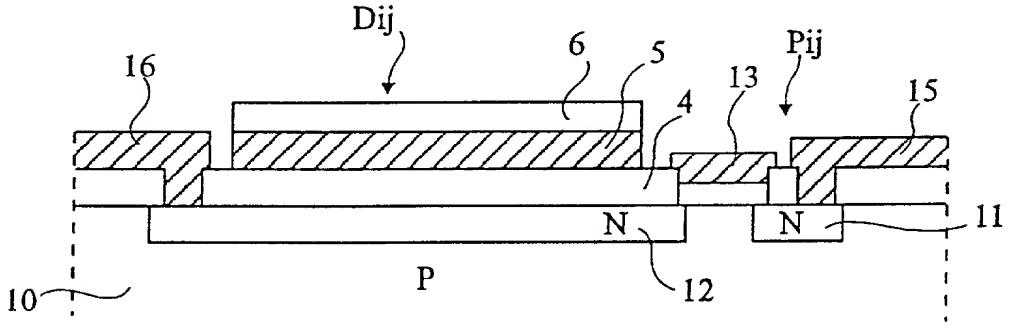

Fig 4